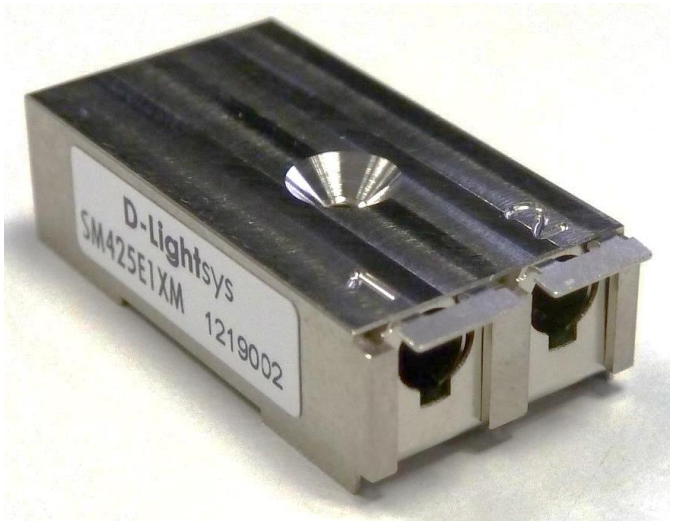
Features

- 1 transmiter and 1 receiver functions
- 0.1-5Gbps per channel
- Suitable for ARINC 818 applications
- Also suitable for IEEE Std. 1000Base-SX, Fibre Channel, Infiniband and VSR requirements.
- Pluggable electrical socket interface
- LuxCis™ / ARINC 801 compatible pluggable optical interface
- Small package size (25 x 13 x 7 mm)
- Low power consumption
- Single 3.3V power supply
- Hot pluggable (plug and play)
- Qualified over the industrial temperature range -40 to +90°C
- Temperature compensation for performance optimization over severe environment range



Applications

- Digital video transmission
- Sensors interconnects
- Radar datacommunication
- Board-to-board communications
- Industrial data links
- Space application
- Severe environment interconnects

Product Description

S-Light SM-425-Ew-XM optoelectronic modules are full duplex transceivers optimized for short distance high data rate optical communication. They are protocol independent and can be applied to Gigabit Ethernet or any balanced network protocols. The S-Light family is optimized for severe environment applications and complies with AEEC / ARINC 804 transceiver specifications.
SM-425-Ew-XM modules integrate state-of-the art 850-nm VCSEL and PIN photodiode chips and low power consumption CMOS electronics.
SM-425-Ew-XM has an optical quick-plug ARINC 801 interface and a plug-in 30 pins electrical interface. SM-425-Ew-XM devices can be tightly screwed to the application board.

Ordering Information

Several versions of pre-series S-Light ESSENTIAL transceivers are currently available.

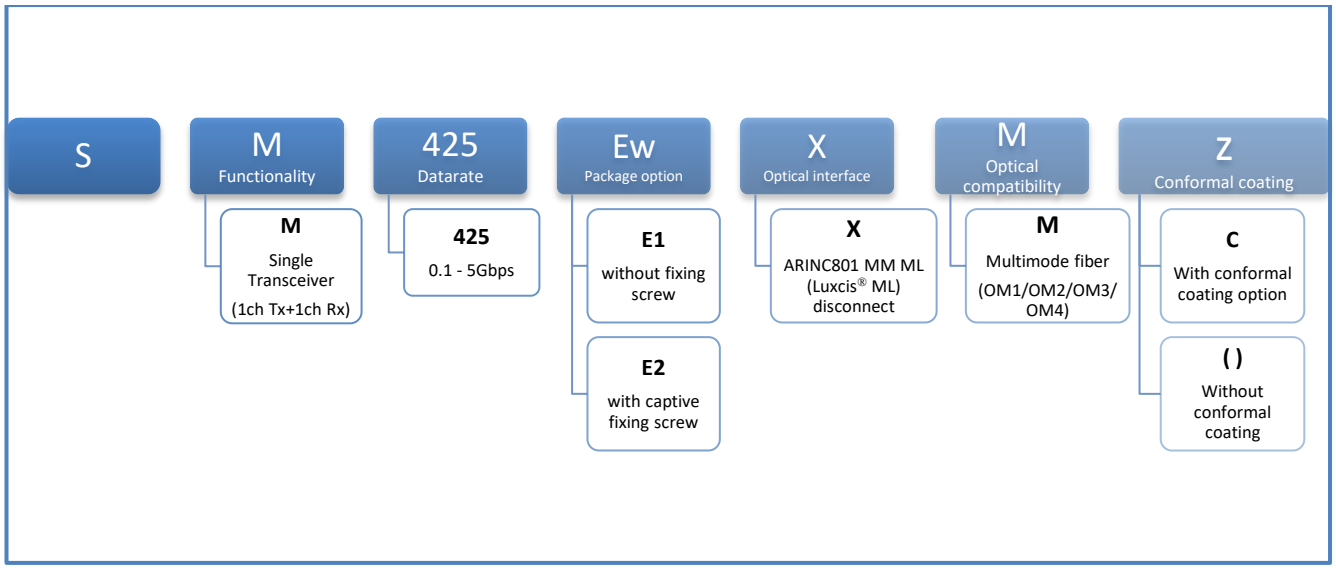


Table of contents

Absolute Maximum Ratings

Stress beyond these values may cause permanent damage to the device.

Table 1 - Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage temperature	T_{st}	-55	+125	°C	-
Supply voltage	V_{CC}	-0.3	+4.0	V	-
Signal pins voltage range	V_{pin}	-0.3	V_{CC}+0.3	V	-
Data input voltage (single ended)	$\|V_{xP}-V_{xN}\|$		1.2	V	-
ESD resistance voltage	ESD	-	2	kV	1

Notes:
1. Human Body Model (HBM) according to JESD22-A114-B.

Module Specifications

Table 2 - General Specifications

Parameter		Symbol	Min	Typ.	Max	Unit	Notes
Supply voltage (V_{CCT}&V_{CCR})		$V_{CCT\&R}$	3.0	3.3	3.6	V	1
Supply current		I_{CC}	-	130	-	mA	-
Power consumption	Dual channel	P_{tot}	-	430	-	mW	2
	Per channel	P_{ch}	-	215	-	mW	2
Data rate per channel		B	0.1	-	5	Gbps	-
Operating temperature		T_{op}	-40	-	+90	°C	-
Optical fiber compatibility				Multimode			3

Notes:
1. V_{CCT}=V_{CCR}=3.3V are recommended for high performances.
2. Power consumption per or for all the channels operating at full speed overall the temperature range for Vccx=3.3V
3. Compatible with multimode fibers (50/125µm & 62,5/125µm)

Table 3 - Transmit Channel High Speed Electrical Specification VCCx=3.3V, VEE=GND=0V, Temp= [-40:+90°C]

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Differential input voltage	V_{INpp}	500	-	1600	mV	1
Input common mode range	V_{xCM}	0.8	1.2	1.7	V	1
Input impedance	Z_{in}	90	100	110	Ω	-
Input capacitance (each input)	C_{in}	-	0.5	-	pF	-

Notes:
1. DC-coupled only

Table 4 - Receiver Channel High Speed Electrical Specification VCCx=3.3V, VEE=GND=0V, Temp= [-40:+90°C]

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Differential output voltage	$\|V_{xP}-V_{xN}\|$	-	400	-	mV	1
Output Rise/Fall Time	t_{outR},t_{outF}	-	50	-	ps	2
Total Jitter	T_J	-	0.15	0.3	UI	3

Notes:
2. Output voltage swing and currents are programmable.
3. Measured at 3.25Gbps and with 20%-80% levels.
4. Measured at 3.25Gbps.

Table 5 - Digital Electrical Specification — VCCx=3.3V, VEE=GND=0V, Temp= [-40:+90°C]

Parameter		Symbol	Min	Typ.	Max	Unit	Notes
Digital input voltage (CMOS)	High	V_{high}	2	-	V_{CC}	V	1
	Low	V_{low}	V_{EE}	-	0.8	V	1
Digital output voltage (CMOS)	High	V_{high}	2.4	-	V_{CC}	V	1
	Low	V_{low}	V_{EE}	-	0.4	V	1
Digital input voltage (Serial, I^2C)	High	V_{high}	2	-	V_{CC}	V	-
	Low	V_{low}	V_{EE}	-	V_{EE}+0.8	V	-
Serial Interface input capacitance		C_I	-	-	10	pF	-
Serial Interface Rise Time		t_r	-	-	1	µs	-

Notes:
1. Compatible with JESD8-B CMOS digital level specifications.

Table 6 - Transmit Channel Optical Specification — VCCx=3.3V, VEE=GND=0V, Temp= [-40:+90°C]

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Center wavelength	λ_c	830	850	860	nm	-
Spectral width – rms	$\Delta\lambda$	-	-	0.65	nm	-
Relative Intensity Noise	RIN	-	-	-128	dB/Hz	
Optical output power	P_{out}	-4	-	+1	dBm	1,2
Optical output power variation over the specified temperature range	ΔP_{out}	-	1	-	dB	-
Optical modulation amplitude	OMA	470		-	µW	-
Optical extinction ratio	E_R	6	9	-	dB	3
Deterministic Jitter	D_J	-	5	20	ps	3
Total Jitter	T_J	-	30	80	ps	3
Rise/Fall time	τ_R, τ_F	-	50	-	ps	4

Notes:
1. Class 1 laser products according to IEC 60825-1/2 standard
2. Output optical power can be adjusted by the user through a 2-Wire serial interface
3. Measured at 3.25Gbps
4. Measured at 20% / 80% levels at 3.25Gbps

Table 7 - Receiver Channel Optical Specification — VCC=3.3V, VEE=GND=0V, Temp= [-40:+90°C]

Parameter		Symbol	Min	Typ.	Max	Unit	Notes
Center wavelength		λ_c	830	850	860	nm	-
Receiver Sensitivity (average power)	1.25Gbps	P_{inMin}	-	-19	-17	dBm	1
	2.5Gbps	P_{inMin}	-	-18.5	-16.5	dBm	1
	4.25Gbps	P_{inMin}	-	-18	-16	dBm	1
	5Gbps	P_{inMin}	-	-17	-15	dBm	1
Unstressed receiver sensitivity (OMA)		P_{inOMA}	-	25	40	µW	2
LOS Optical threshold		LOS_{TH}	-	-22.5	-	dBm	-
LOS Optical hysteresis		LOS_{HYS}	-	2.5	-	dB	-
Optical return loss		RL	12	-	-	dB	-

Notes:
1. For a 10^{-12} BER with a PRBS 2^7-1
2. Data rate : 4.25Gbps

Functional Block Diagram

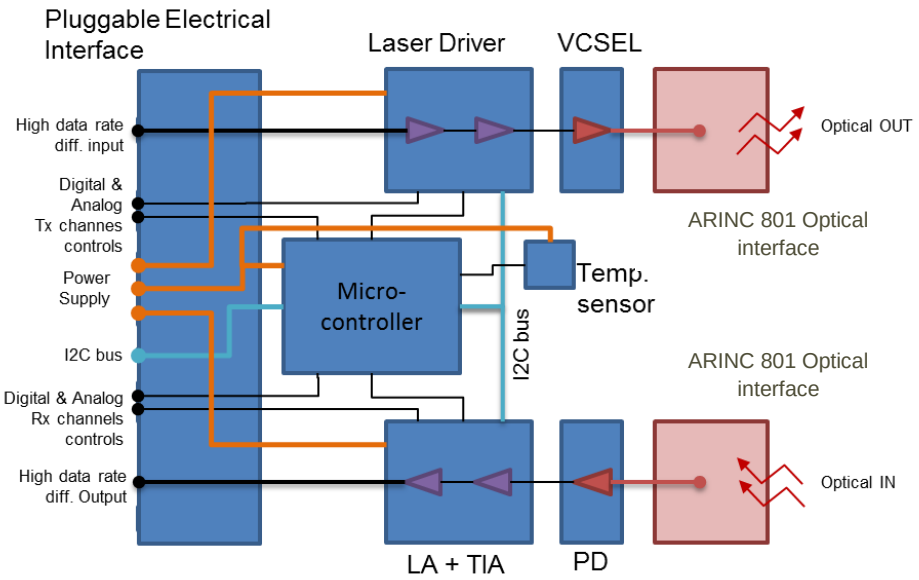


Fig.1 - Functional Block Diagram (from bottom side)

Memory organisation

<table>
<tr><th>I²C Memory Location (Hex) SRAM</th><th>Function Description
Values by default can be changed without notice</th></tr>
<tr><td rowspan="2">01h</td><td>
RX Controls (Default = x111 110x)
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Res</td><td>LOS_EN</td><td>LOS_POL</td><td>RX_POL</td><td>SQ_EN</td><td>RX_EN_STATUS</td><td>RXDE_EN</td><td>Res</td></tr>
</table>
Bit 6: LOS_EN. Controls the LOS & LLOS circuitry. When RX_EN is set to 0, the LOS detector is also disabled.
0 = disabled/1 = enabled
Bit 5: LOS_POL. Controls the output polarity of the LOS pin. 0 = inverse / 1 = normal
Bit 4: RX_POL. Controls the polarity of the receiver signal path. 0 = inverse / 1 = normal
Bit 3: SQ_EN. When SQ_EN = 1, the LOS controls the output circuitry. 0 = disabled / 1 = enabled
Bit 2: RX_EN_STATUS.(Read only) Indicates the state of Rx enable. (0 = Rx disabled / 1 = Rx enabled).

If pin RxEn is connected to GND or Rx_En=0, then Rx output circuitry is disable and Rx_EN_STATUS=0
<table>
<tr><td></td><td>Rx En Pin = GND*</td><td>Rx En Pin = VCC or NC*</td></tr>
<tr><td>Rx_En Register (012h, bit2) = 0</td><td>Rx_En_Status = 0 – Rx disable</td><td>Rx_En_Status = 0 – Rx disable</td></tr>
<tr><td>Rx_En Register (012h, bit2) = 1</td><td>Rx_En_Status = 0 – Rx disable</td><td>Rx_En_Status = 1 – Rx enable (normal operation)</td></tr>
</table>
* With RX_EN_INVERT register = 0

Bit 1: RXDE_EN. Enables or disables the deemphasis on the receiver output. 0 = disabled / 1 = enabled
</td></tr>
<tr><td>02h</td><td>
RX Status (latched)
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Res</td><td>Res</td><td>Res</td><td>Res</td><td>Res</td><td>Res</td><td>Res</td><td>LLOS</td></tr>
</table>
Bit 0: LLOS. Latch Loss Of Signal. The first 0-to-1 transition gets latched until the bit is cleared (write 0 or use reset).
</td></tr>
<tr><td>03h</td><td>
RX Output CML Level Setting Register (Default = 0101 0011)
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>SET_CML[7]</td><td>SET_CML[6]</td><td>SET_CML[5]</td><td>SET_CML[4]</td><td>SET_CML[3]</td><td>SET_CML[2]</td><td>SET_CML[1]</td><td>SET_CML[0]</td></tr>
</table>
The SET_CML register is an 8-bit register that can be set up to 255, corresponding to an output up to 1000mVP-P.
CML output amplitude (mVpp) ~ 4,9*SET_CML[7:0] + 60
</td></tr>
<tr><td>05h</td><td>
TX Controls (Default = xxxx 0001)
<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Res</td><td>Res</td><td>Res</td><td>Res</td><td>TXDE_EN</td><td>Res</td><td>TX_POL</td><td>TX_EN_STATUS</td></tr>
</table>
Bit 3: TXDE_EN. Enables or disables the transmit output deemphasis circuitry. 0 = disabled / 1 = enabled
Bit 1: TX_POL. Controls the polarity of the transmit signal path. 0 = normal / 1 = inverse
Bit 0: TX_EN_STATUS. (Read only) Indicates the state of Tx output. (0 = disabled (VCSEL OFF) / 1 = enabled (VCSEL ON))

If pin TxEn is connected to GND or Tx_En=0, then Tx circuitry is disable and Tx_EN_STATUS=0
<table>
<tr><td></td><td>Tx En Pin = GND*</td><td>Tx En Pin = VCC or NC*</td></tr>
<tr><td>Tx En Register (012h, bit3) = 0</td><td>Tx_En_Status = 0 – VCSEL OFF</td><td>Tx_En_Status = 0 – VCSEL OFF</td></tr>
<tr><td>Tx En Register (012h, bit3) = 1</td><td>Tx_En_Status = 0 – VCSEL OFF</td><td>Tx_En_Status = 1 – VCSEL ON (normal operation)</td></tr>
</table>
* With TX_EN_INVERT register = 0
</td></tr>
</table>

06h

TX Fault Register (latched)

7	6	5	4	3	2	1	0
Res	Res	Res	Res	Res	Res	Res	TX_FAULT

TX_FAULT indicates a default on Tx circuitry like:
- Really low voltage on VCCT pin (<2.5V)
- Abnormal VCSEL Voltage
- Too important/low bias current into the VCSEL
- Too important bias current increase

It may disable the output circuitry.
In case of Tx_Fault please contact sales.

The Tx Fault register can be cleared with CLEAR_FAULTS register.

0Fh

TX Pulse-Width Control Register (Default = xxxx 0000)

7	6	5	4	3	2	1	0
Res	Res	Res	Res	SET_ PWCTRL[3] (MSB)	SET_ PWCTRL[2]	SET_ PWCTRL[1]	SET_ PWCTRL[0] (LSB)

Bits 3 to 0: SET_PWCTRL[3:0]. This is a 4-bit register used to control the eye crossing by adjusting the pulse width.

10h

TX Deemphasis Control Register (Default = xxxx 0000)

7	6	5	4	3	2	1	0
Res	Res	Res	Res	SET_ TXDE[3] (MSB)	SET_ TXDE[2]	SET_ TXDE[1]	SET_ TXDE[0] (LSB)

Bits 3 to 0: SET_TXDE[3:0]. This is a 4-bit register used to control the amount of deemphasis on the transmitter output. When calculating the total modulation current, the amount of deemphasis must be taken into account. The deemphasis is set as a percentage of modulation current.

11h

Command Register 1 (CMD1 - Default = xxxx0xx0)

7	6	5	4	3	2	1	0
Res	Res	Res	Res	WRITE_ FLASH	Res	Res	MANUAL

Bit3: WRITE_FLASH. See Flash memory guidelines section for more details

Bit0: MANUAL:

Manual = 0: Normal operation mode – VCSEL temperature compensation activated.

Manual = 1: For modification of parameters - VCSEL temperature compensation desactivated. See Flash memory guidelines section for more details

12h

Command Status Register 2 (CMD2)

7	6	5	4	3	2	1	0
WRITE_ ENABLE	RESTORE	LOS	RESET	TX_EN	RX_EN	CLEAR_FAU LTS	Res

Bit7: Write Enable. See Flash memory guidelines section for more details.

Bit6: RESTORE: Put WRITE_ENABLE to 1 and then RESTORE to 1. This will restore all RADIALL default parameters (after reboot).

Bit5: LOS. Rx Loss Of Signal – Reflects the LOS pin status.

Bit4: RESET: Load all parameters saved into the flash (same effect as reboot).

Bit3: Tx_EN : To disable the Tx circuitry (0:disable / 1:enable if Tx1 En pin NC or VCC).- Cf register 05h for more information

Bit2: Rx_EN : To disable the Rx circuitry (0:disable / 1:enable if Rx1 En pin NC or VCC).- Cf register 01h for more information.

Bit1: CLEAR_FAULTS : Reset fault register (if default is not present anymore)

13h

Command Register 3 (CMD3 - Default = 00xx xxxx)

7	6	5	4	3	2	1	0
TX_EN_INVE RT	RX_EN_INVE RT	Res	Res	Res	Res	Res	Res

Bit7: TX_EN_INVERT. Invert TX_EN **pin** logic. See Flash memory guidelines section for more details

Bit6: RX_EN_INVERT. Invert RX_EN **pin** logic. See Flash memory guidelines section for more details

14h	**Temperature Digital Register**							
	7	6	5	4	3	2	1	0
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	The temperature register is a two's complement integer rounded to the nearest degree °C. These registers indicate approximate environment temperature.							
15h	**Imon Digital Register (2 Bytes)**							
	7	6	5	4	3	2	1	0
	Res	Res	Res	Res	Res	Res	Bit 9	Bit 8
16h	7	6	5	4	3	2	1	0
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	The Imon monitor voltage is a 10 bit integer proportional to the current injected into the VCSEL. The typical link between the value read in these registers and the bias current injected in the VCSEL is the following: $Imon_{(dec)} \sim 61*Ibias_{(mA)}$.							
17h (MSB)	**RSSI Digital Register (2 Bytes)**							
	7	6	5	4	3	2	1	0
	Res	Res	Res	Res	Res	Res	Bit 9	Bit 8
18h (LSB)	7	6	5	4	3	2	1	0
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	The RSSI digital register is a 10 bit integer proportional to received RX signal. The typical link between the value read in these registers and the input optical power is the following: $RSSI_{(dec)} \sim 200*Pin_{(mW)}$.							
19h-1Ch	**Part Number Code**							
	These 4 bytes encode the manufacturing part number for the device.							
1Dh-20h	**Serial Number Code**							
	These 4 bytes encode the unique manufacturing serial number given to each module.							
21h	**D-Lightsys Device ID (Default = 0xE1)**							
	This is the general device ID for the Sx-425-Ex-XM. This value can be used for device identification and is written to this register once during power up. This value can be overwritten and is volatile.							
22h	**Firmware Version**							
	This byte will display the firmware version of the module. The version is the hex value converted to decimal and placed in a x.x.x format. For example a hex value of 73h would be 115 in decimal and would correspond to version 1.1.5							
23h	**I^2C Address (Default = 0x50)**							
	Transceiver I^2C address can be adjusted with this 8 bits register							

Flash memory guidelines

Saving Controls/Driver Configurations to Flash Memory

To be able to write the configuration to flash, there is a sequential procedure:

- Set write enable : CMD2 bit7 = 1
- Update configuration of desired registers in the following list :
  - Register 01h – 10h (Red registers in Memory organization section) – Need CMD1 bit0 = 1
  - I2C Address (23h)
  - TX_EN_INVERT / RX_EN_INVERT (13h)
- Set Write : CMD1 bit3 = 1
- Wait for CMD1 bit3 = 0

Please note that during a write, the current state of registers 01h-10h are saved to flash.

Package mechanical drawings

These dimensions are given for information (in mm).

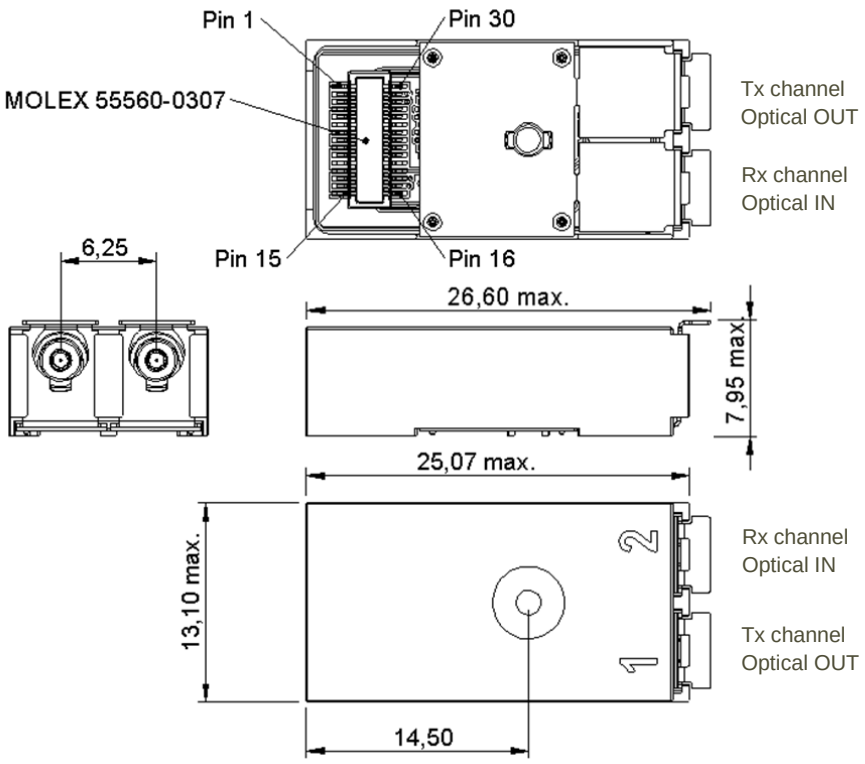


Fig.2 - Package mechanical drawing

Application board electrical pinout

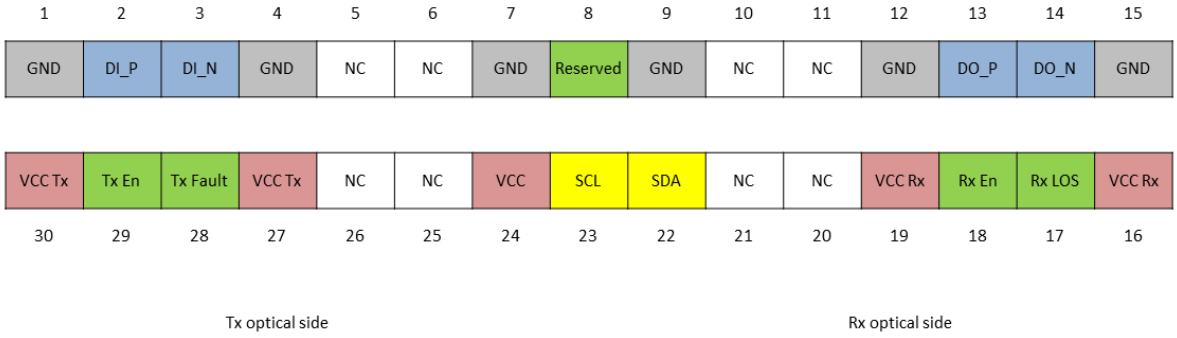


Fig.3 - Single channel transceiver pinout (viewed from top)

Pin out description

Signal	Pin number	Type	Description
GND	1,4,7,9,12,15	Power	**Negative supply rail:** negative power supply tied to GND (0 Volt)
DI_P or DataIn+	2	High Speed Input	**Positive Data input for Tx channel**: LVDS/CML positive high speed input
DI_N or DataIn-	3	High Speed Input	**Negative Data input for Tx channel**: LVDS/CML negative high speed input
NC	5,6,10,11 20,21,25,26	-	**Not connected Pins**: Do not connect those pins.
Reserved	8	-	**Reserved pin**: Do not connect this pin. For manufacturing test purpose or future development options
DO_P or DataOut+	13	High Speed Output	**Positive Data output for Rx channel**: LVDS/CML positive high speed output
DO_N or DataOut-	14	High Speed Output	**Negative Data input for Rx channel:** LVDS/CML negative high speed output
Vcc Rx	16, 19	Power	**Positive supply rail for the receiver stage**: +3.3Volts positive power supply
Rx LOS	17	Digital output (Strong)	**Rx Loss of Signal Output**: The default polarity of LOS is high when the level of the input signal is below the threshold. **Need RF modulation to be active**
Rx En	18	Digital Input Pull-up	**Receiver Enable**: Enable/Disable the Rx output circuitry. When Low the electrical data output is turned OFF. Default is RxEnable High (normal operation, output activated).
SDA	22	Digital In/output (Open Drain)	**2-Wire serial data interface**: The serial data pin is for serial data transfer to and from the module. The pin is open drain and may be wired-OR with other open drain or open collector interfaces. Can be connected to GND if not used
SCL	23	Digital Input (Open Drain)	**2-Wire Serial Clock input**: The serial clock input is used to clock data (SDA pin) into the module controller memory on rising edges and clock data out on falling edges. Can be connected to GND if not used
Vcc	24	Power	**Positive supply rail for the microcontroller stage**: +3.3Volts positive power supply
Vcc Tx	27,30	Power	**Positive supply rail for the transmitter stage**: +3.3Volts positive power supply.
Tx Fault	28	Digital output (Strong)	**Image of TX_FAULT status bit:** The polarity of Int Tx1 is high when TX_FAULT bit = 1(Int Tx1 is high when an error occur, Tx1 is low during normal operation.)
Tx En	29	Digital Input Pull-up	**Transmitter Enable**: Enable/Disable the module lasers. When Low the laser is turned OFF. Default is TxEnable High (normal operation, laser turned ON).

Package mechanical drawings with ARINC 801 contact *

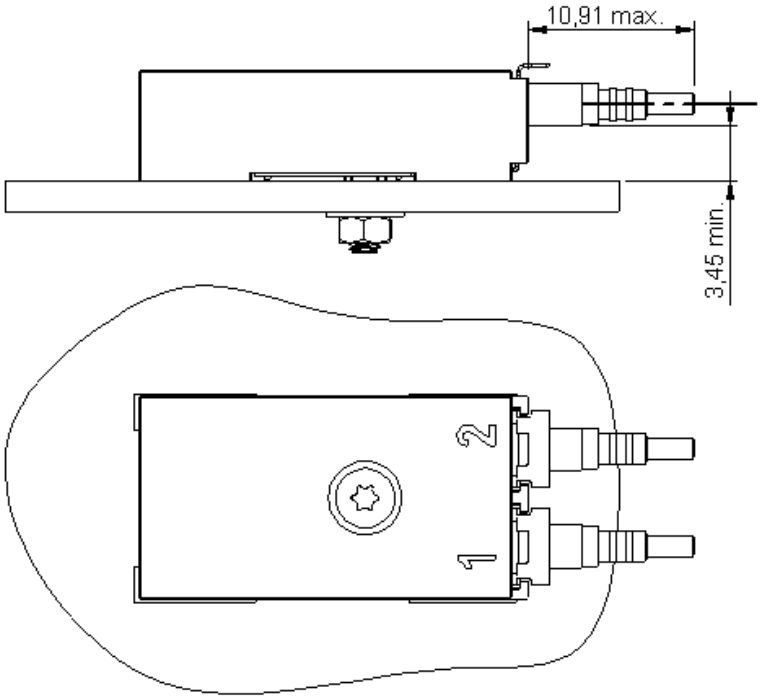


Fig.4 - View of the package mounted on PCB with connected LuxCis

* Use only **Luxcis® MM ML** contact for loose structure optical cable (ARINC801 LM)

Mechanical fixture

Two mounting options are proposed to hold down the module on the application board;

- screwing from top side by means of captive screw integrated within Essential package (Fig 5)
- screwing from rear side with customer selected fixture (Fig 6)

See AN-SLM15 for more details.

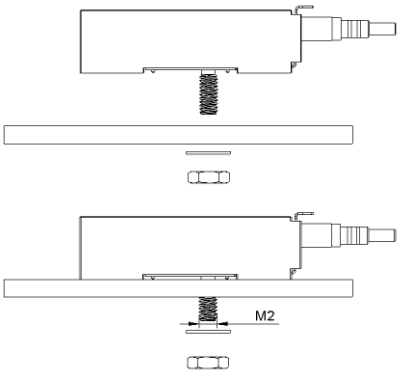


Fig.5 - Screwing from top side with captive screw (1)

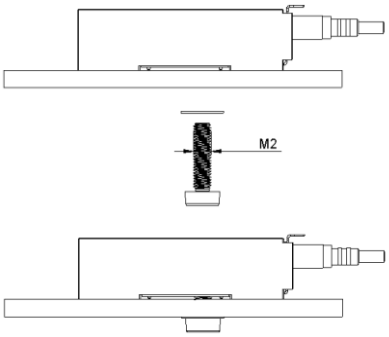


Fig.6 - Mounting from rear side

(1) To be ordered as SM-425-E**2**-XM

Recommended PCB layout

The PCB layout is viewed from above.
These dimensions are given for information (in mm).

It is strongly recommended to route RF signals on internal layers to improve EMI susceptibility. Radiall suggest using vias between the 2 pins arrays of the electrical connector.

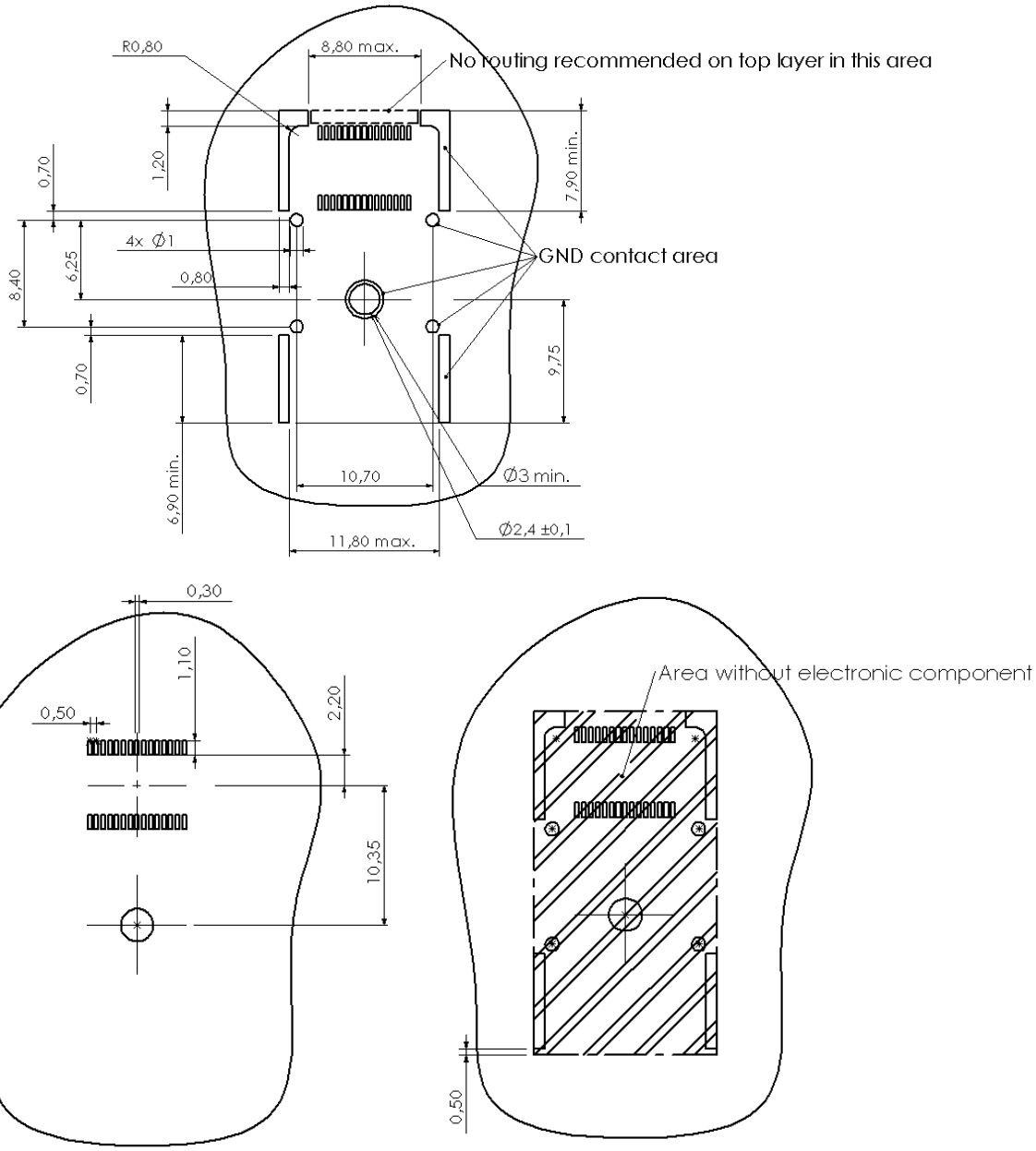


Fig.7 - Recommended PCB layout

Qualification summary

Test	Standard	Conditions
Qualified temperature range	ARINC804	Up to [-40;+90°C]
Low temperature endurance	ARINC804	Up to 1000h @-40°C
High temperature endurance	ARINC804	Up to 2000h @90°C
Rapid change of temperature	MIL-STD-883	Up to -55/+125°C, 500 cycles, 8°C/ min., dwell time: 10min.
Thermal shock	MIL-STD-883	Up to -40/+100°C x15 - 30 min dwell time
Vibration	MIL-STD-883	20g Y axis, 9g X&Z axis 1 hour/axis
Mechanical shock	MIL-STD-883	Up to 1500g peak, 0.5ms, 5x per orientation
Damp heat	ARINC804	Up to 500h @40°C HR 95%
Optical mating cycles	-	50 mating/unmating
Electrical mating cycles	-	30 mating/unmating

Library

All these documents are available on request.

AN-SLM15: Essential kit user guide
EVB_SM425E-V1: Essential evaluation board datasheet

Document history

Version	Date	Author	Signed-off	Notes
V0.0	10/15/2018	RS, FQ	LP	Draft document
V0.0	13/12/2019	AC	LP	Update of the power consumption and spectral width
V0.0	27/01/2020	VF	AC	Update of the figures 5/9, table 4/6/7, minor corrections
V1.0	10/01/2020	VF	LP	Official release
V1.1	28/02/2020	VF	LP	Minor corrections
V1.2	17/06/2020	AC	VF	PCB routing recommendations Memory table RSSI description RX LOS changed from Open Drain to Strong Add conformal coating option in PN Improvement of the sensitivity (Table 7)
V1.3	13/01/2021	AC, SP	VF	Registers description clarification Inversion of registers SN/PN No SFF 8472 compatible Upgrade maximum datarate Upgrade maximum operational temperature Remove option 1 & 4 from mounting options
V1.4	24/06/2021	AC	VF	Qualification summary RxInt strong drive Update initial values of RX_POL Change TxInt management Add backup/restore & reset (factory reset feature) Update TX_EN and RX_EN with pins and PSOC registers Add clear faults functionality Status : Pre-series