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## Layout Considerations for ST60 Antennas

Customer : **GENERIC**

Project : **GENERIC PCB (FR4, 4 Layers, Development PCB)**

### Reference documents:

Document Name	Document Type	Description / Comments
R380.845.002 - - A EN.pdf	T.D.S.	H-Polarization Gold Plated LCP Horn Antenna / Commercial Range
R380.845.102 - - A EN.pdf	T.D.S.	V-Polarization Gold Plated LCP Horn Antenna / Commercial Range
R380.846.002 - - A EN.pdf	T.D.S.	H-Polarization Gold Plated LCP Horn Antenna / Industrial Range
R380.846.102 - - A EN.pdf	T.D.S.	V-Polarization Gold Plated LCP Horn Antenna / Industrial Range
201910575-10-0_24-10-19A.DXF.zip	DXF Files	H-Polarization Horn Antenna Footprint
201910575-10-1_24-10-19A.DXF.zip	DXF Files	V-Polarization Horn Antenna Footprint

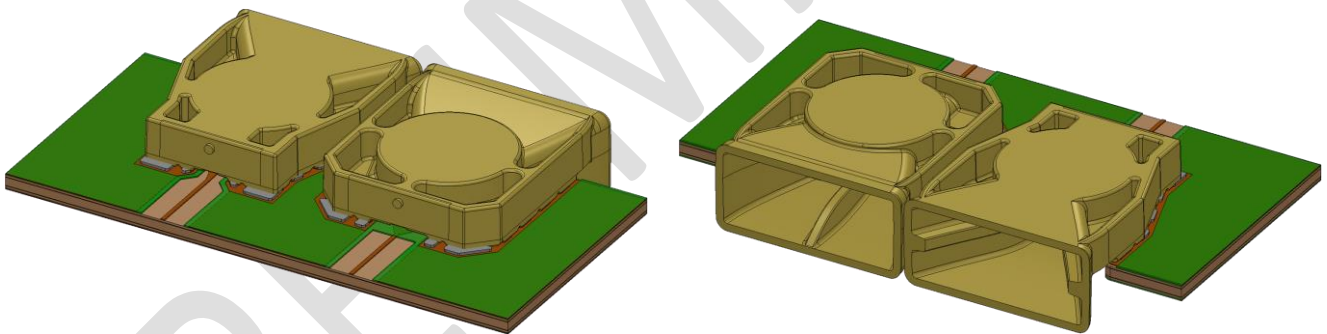
### Content:

This document is intended as a reference for the layout design when using the Stackup shown in table 1.

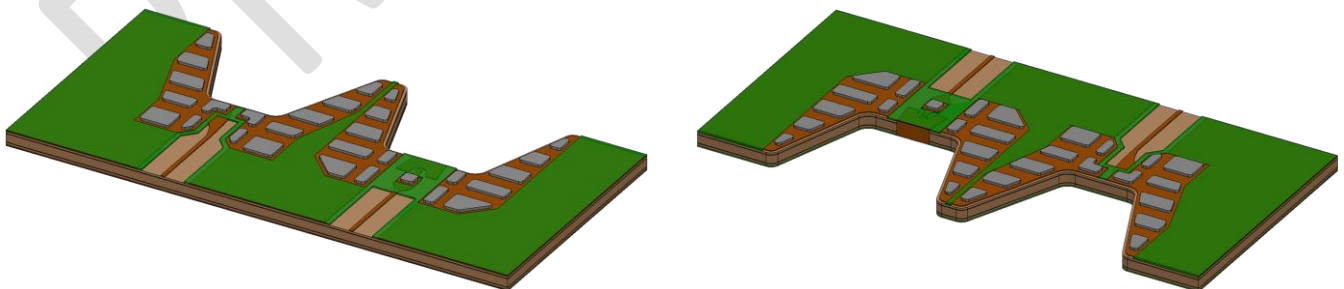
**Please note that the transition from the PCB to the antenna is performance critical. Any modification to the PCB stackup and / or board layout may result in RF performance degradation, and therefore should be assessed.**

The ST60 chips and antennas are mm-wave devices. General microwave design rules should be applied to design the complete board (and the areas comprising the ST60 chips and antenna in particular) in order to avoid crosstalk and resonance phenomena. Particular attention shall be paid to plated through hole locations, line characteristic impedance, and sharp discontinuities.

In the following layout antennas are placed on the top layer



*Figure 1: View of the Antennas Soldered on the PCB*



*Figure 2: Views of the PCB (PSR TOP shown in green)*

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## Associated PCB Stackup:

The PCB is a 4 copper layers stackup, 0.63mm thick with plated thru holes.

	Material <i>(For information Only)</i>	Er <sup>(1)</sup>	TanΔ	Thickness (μm) <sup>(2)</sup>
ENIG plating				4
Solder mask	Probimer 77	4 @ TBD		20
Copper 1				35
Core	IT 158	4.1 @ 5GHz	0.018 @ 5GHz	70 <sup>(3)</sup>
Copper 2				18
Prepreg	IT 158	4.1 @ 5GHz	0.018 @ 5GHz	319
Copper 3				18
Core	IT 158	4.1 @ 5GHz	0.018 @ 5GHz	70 <sup>(3)</sup>
Copper 4				35
Solder mask	Probimer 77	4 @ TBD		20
ENIG plating				4
<b>TOTAL :</b>				<b>613</b>

*(1): Dielectric Constant Tolerance: ±10%*

*(2): Thickness Tolerance: ±10%*

*(3): Works with 81μ Nominal Thickness Cores*

Table 1: PCB Stackup

### PCB characteristics

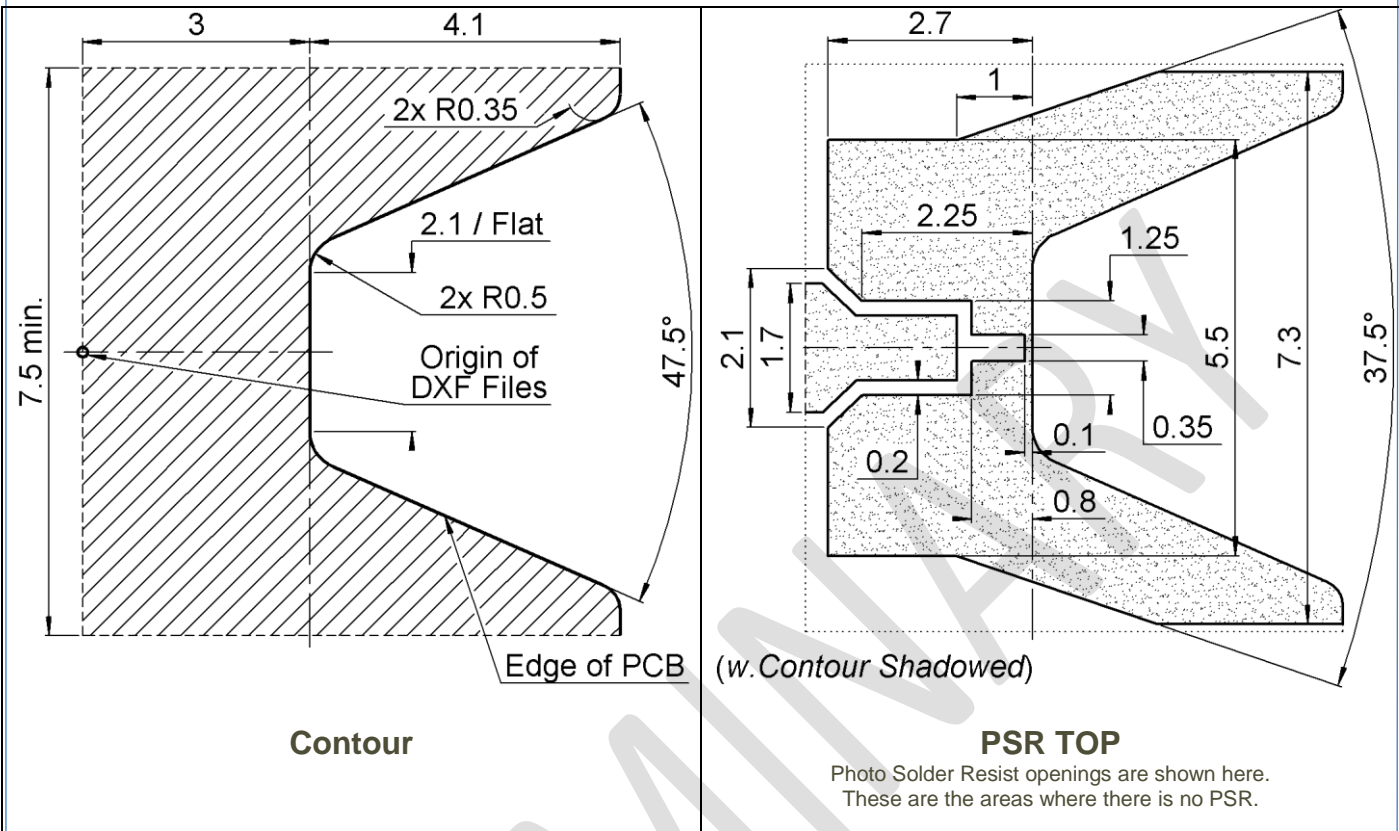
- Copper :
  - Min track width / spacing : 0.12mm
  - Tolerance : +/- 40um
  
- Vias :
  - Plated Thru Holes
  - Drill diameter : 0.2mm
  - Pad diameter : 0.45mm (*inner and outer layers*)
  - Plugged vias (*to control the quantity of solder paste on the pads surface*)
  - Via stitching : 0.5mm pitch typ. (*0.7mm max*)
  
- Surface finish: ENIG plating without solder mask is suggested on the transmission lines to minimize losses between chips and antennas.

The antennas are 1 port component (*pad location is indicated below, p. 5 and 8*). The pad is where the track coming from the chip will be attached.

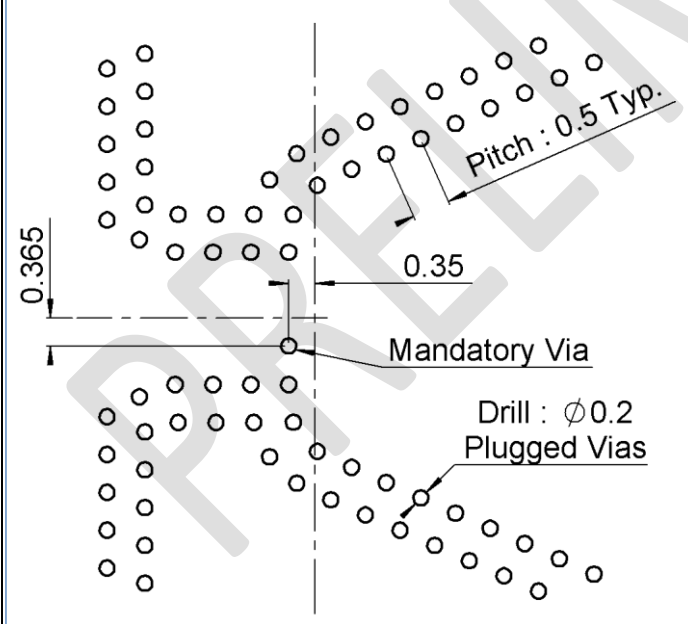
If required by your PCB design tool, you might need to add 1 port for each ground via (*in the pads*) so they are part of the component footprint.

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### H-Polarization Horn Antenna:

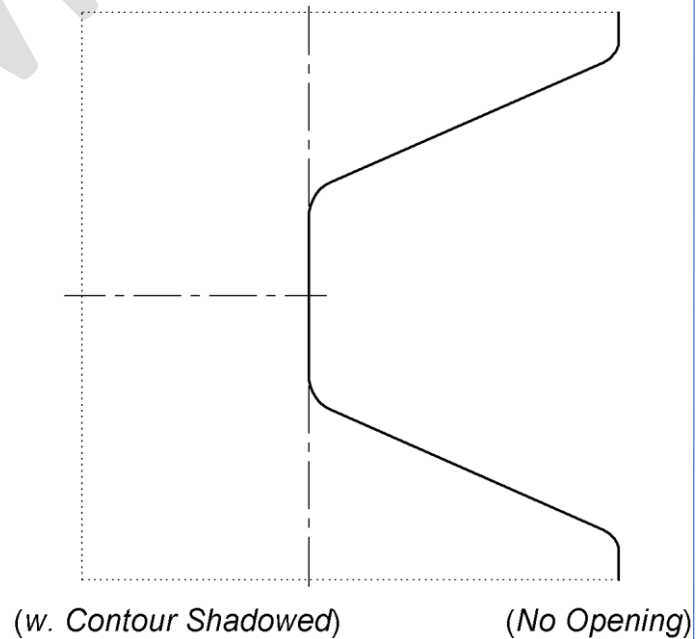


2 rows of vias, @ 0,5 Typ. pitch, placed as defined ( for at least 1 hole), or as close as possible to the edges of the copper layers.



### VIAS

The via marked as "mandatory" shall not be suppressed or moved. For the other vias, we recommend a 0.5mm pitch stitching on two rows

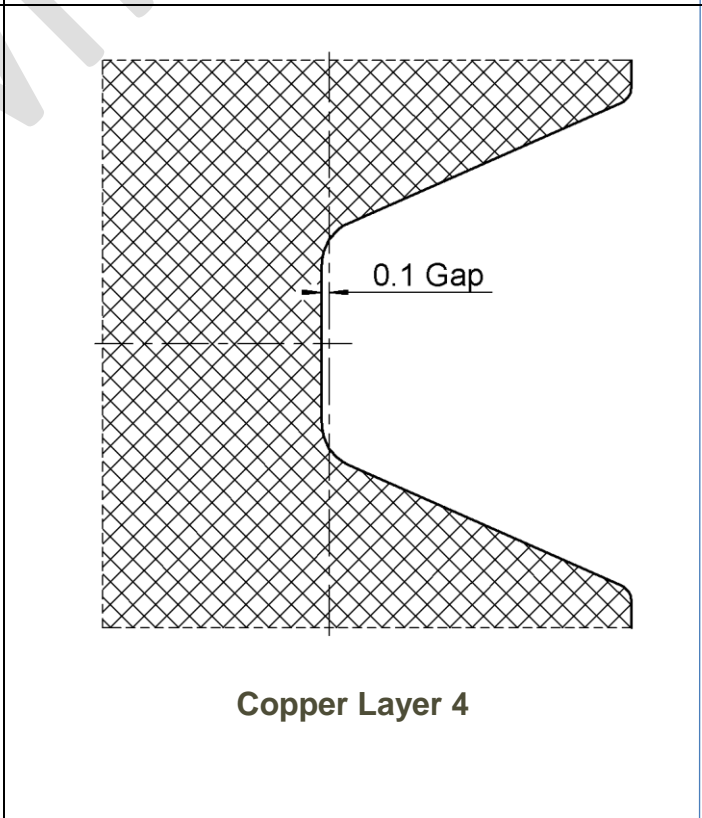
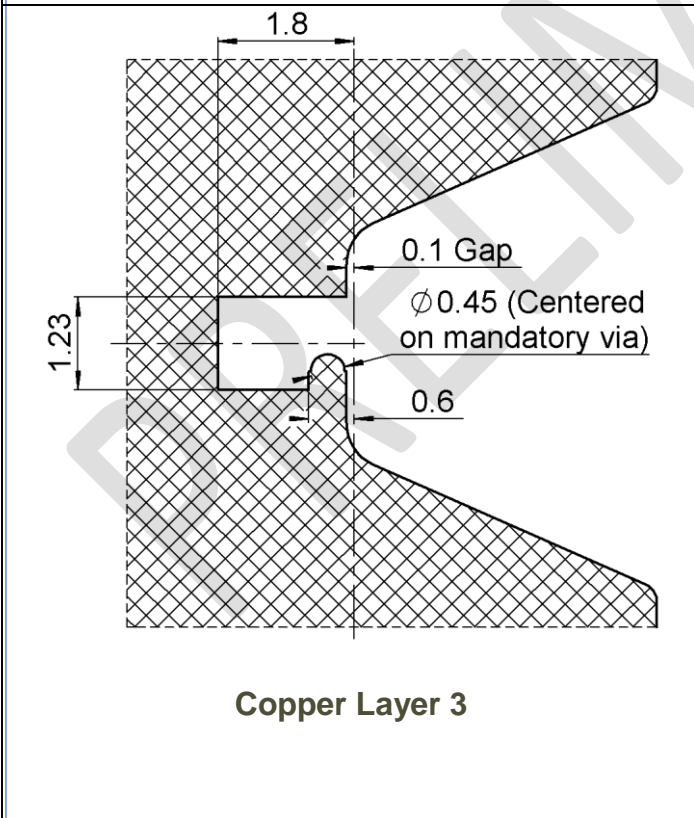
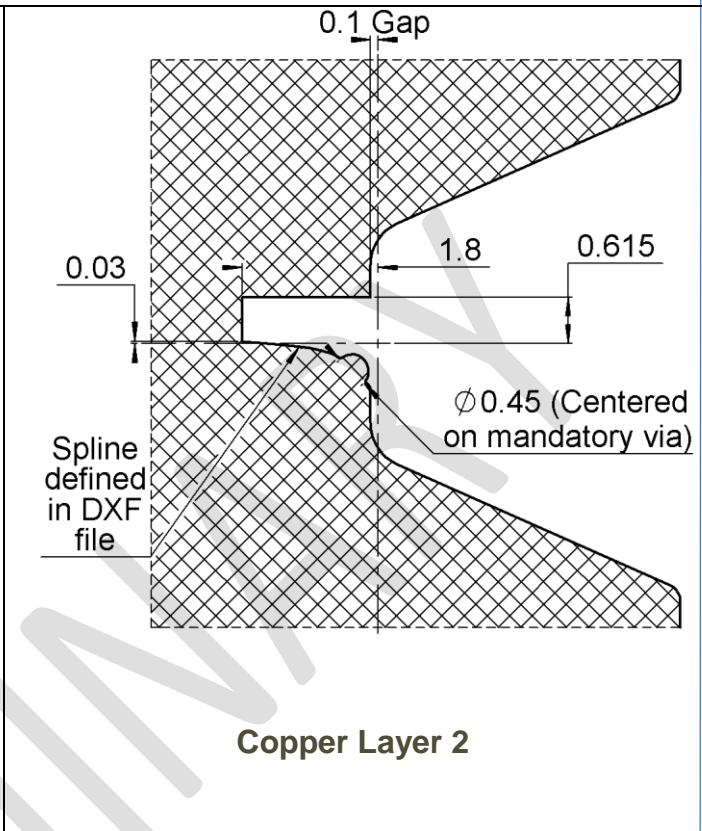
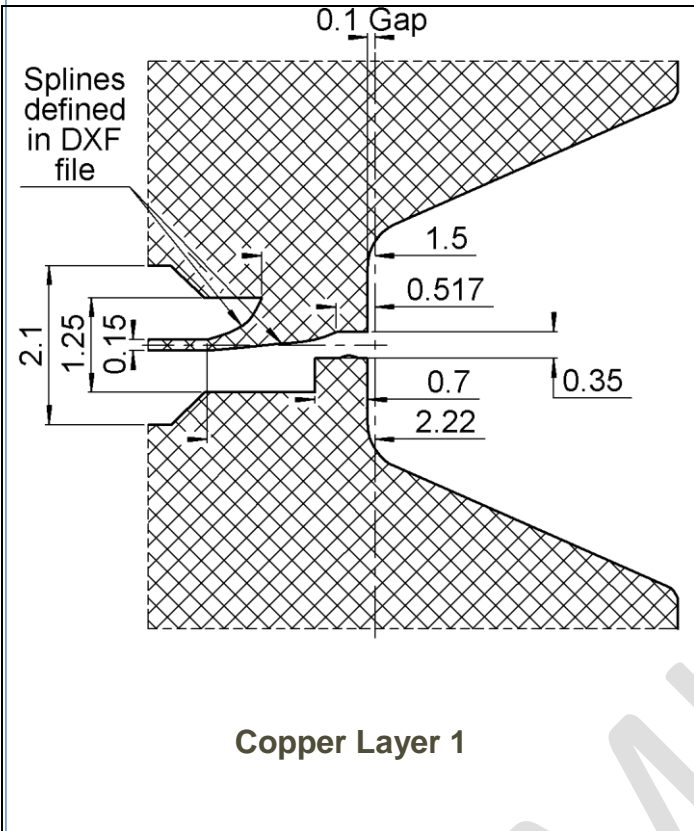


### PSR BOTTOM

In the antenna area, bottom is fully covered by PSR.

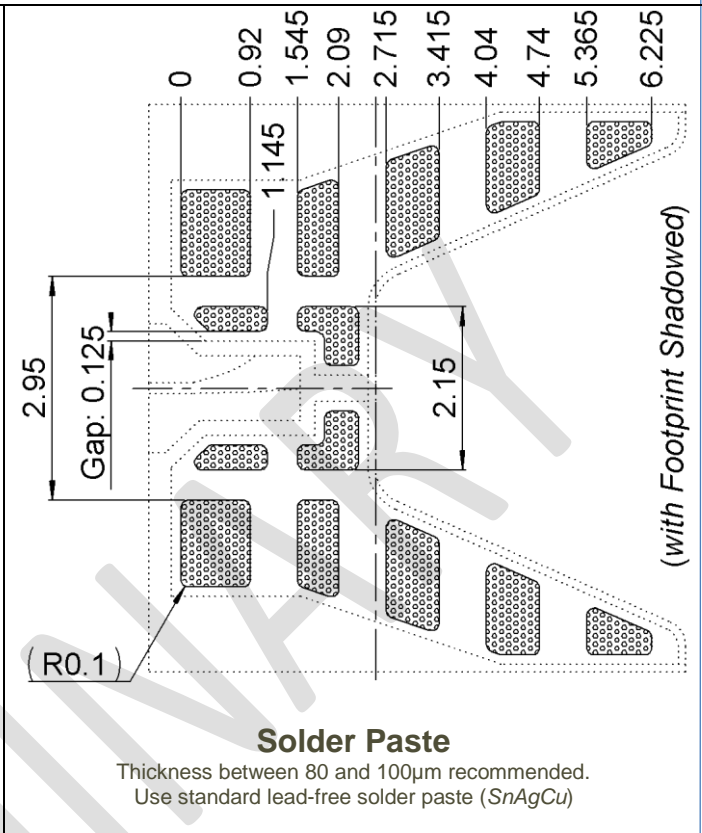
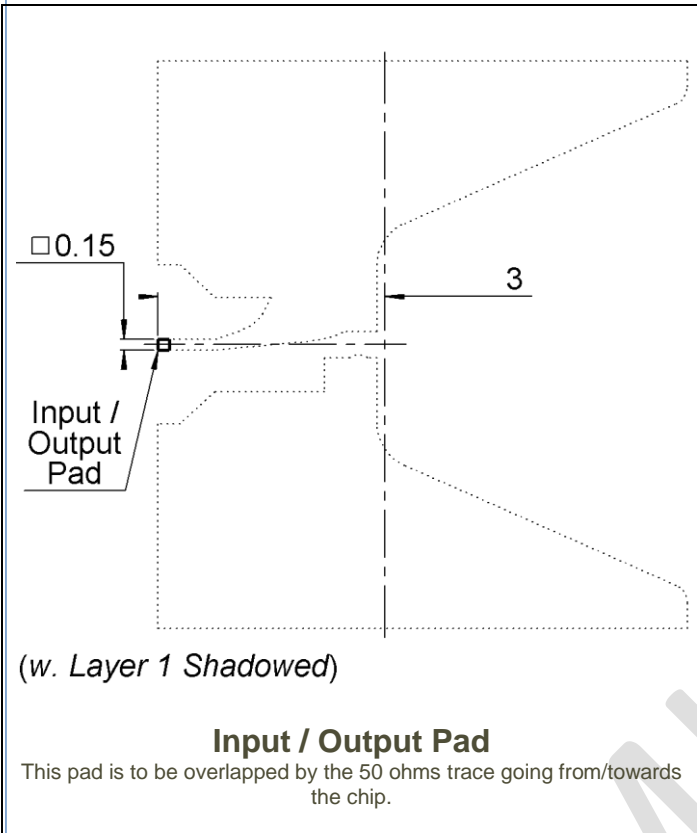
----- : The layer can expand beyond the footprint limit

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----- : The layer can expand beyond the footprint limit

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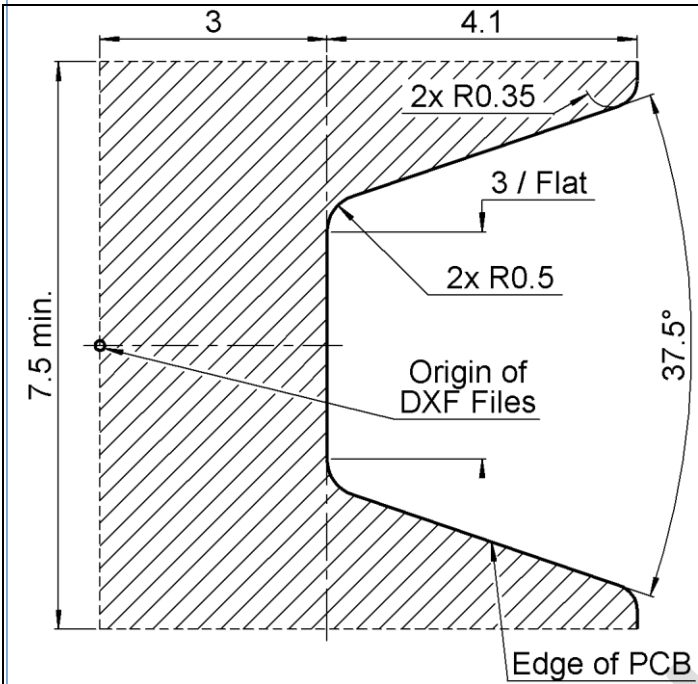


----- : The layer can expand beyond the footprint limit

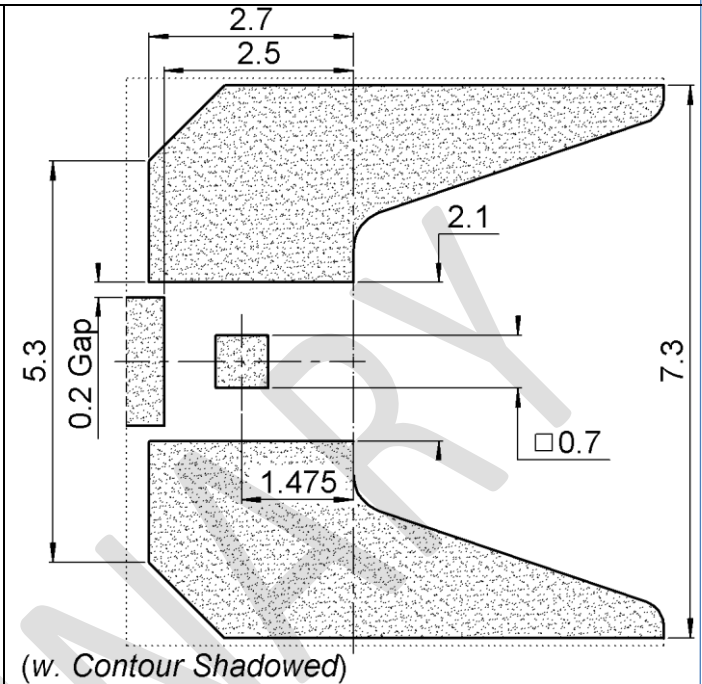
PRELIMINARY

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**V-Polarization Horn Antenna:**



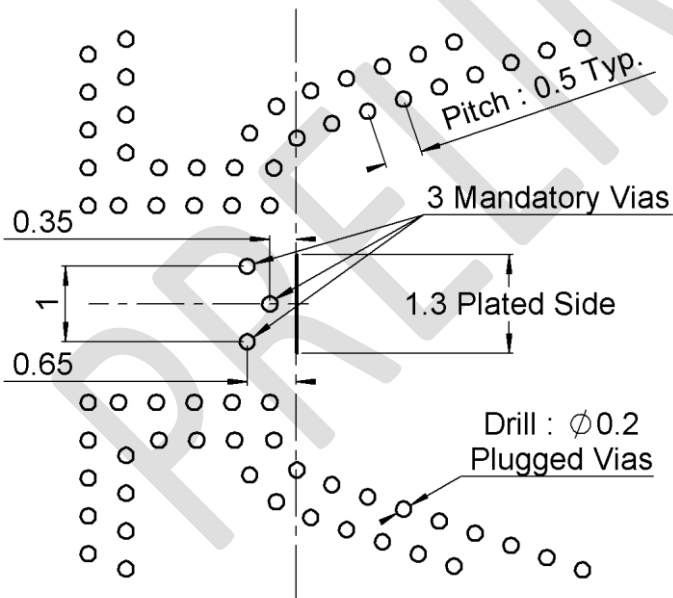
**Contour**



**PSR TOP**

Photo Solder Resist openings are shown here. These are the areas where there is no PSR.

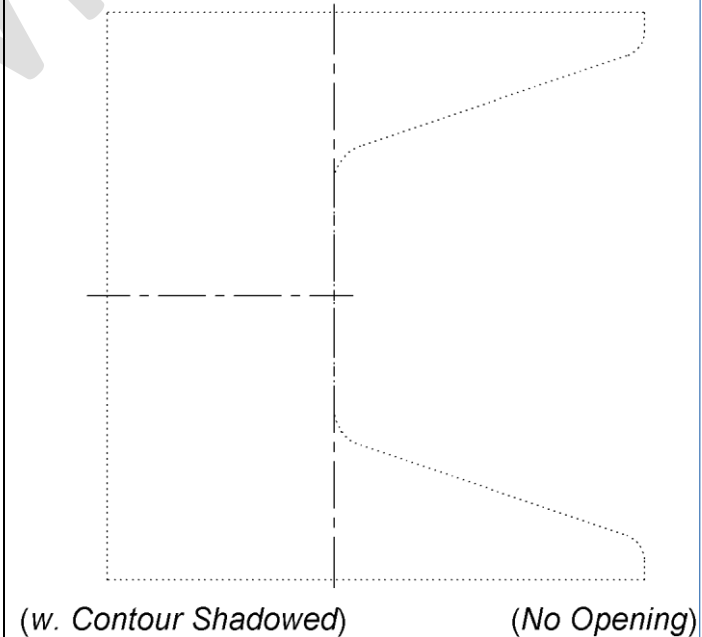
2 rows of vias, @ 0,5 Typ. pitch, placed as defined ( for at least 3 holes), or as close as possible to the edges of the copper layers.



**VIAS**

Plated side on all layers is required locally for this antenna reference. The vias marked as "mandatory" shall not be suppressed or moved. For the other vias, we recommend a 0.5mm pitch stitching on two rows

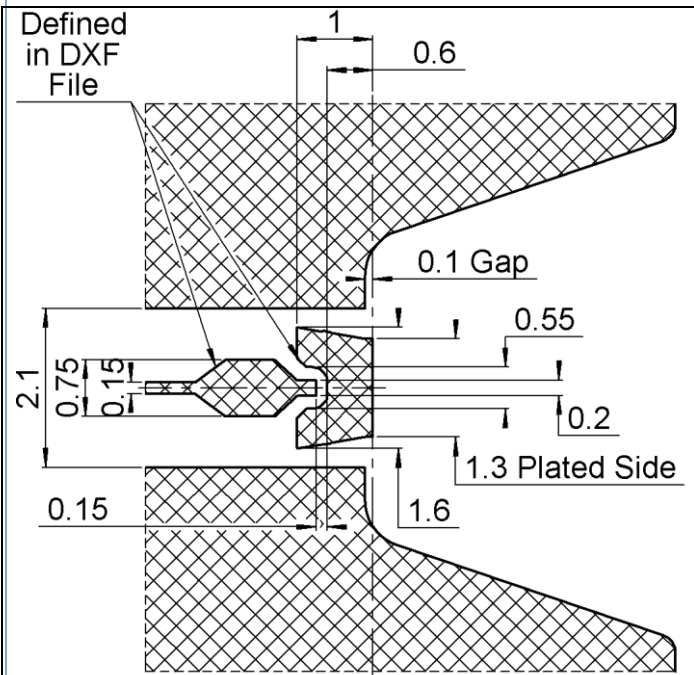
----- : The layer can expand beyond the footprint limit



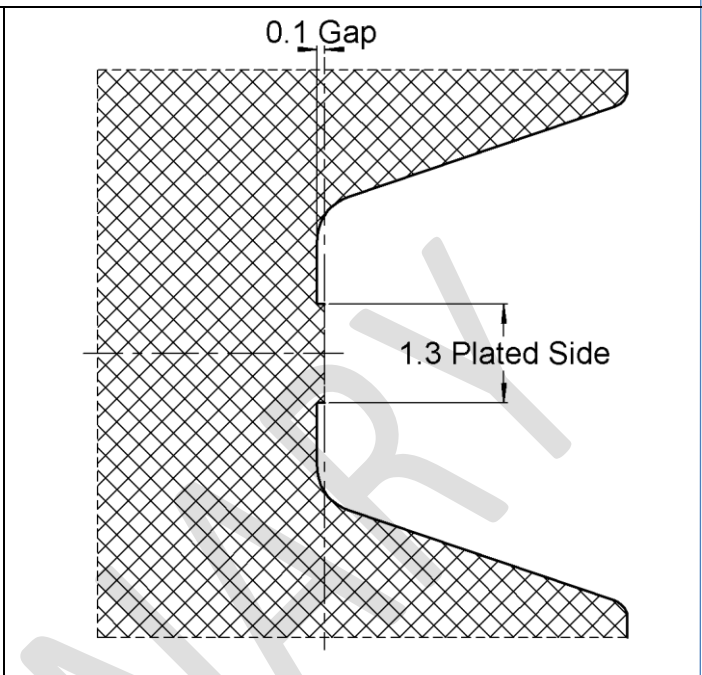
**PSR BOTTOM**

In the antenna area, bottom is fully covered by PSR.

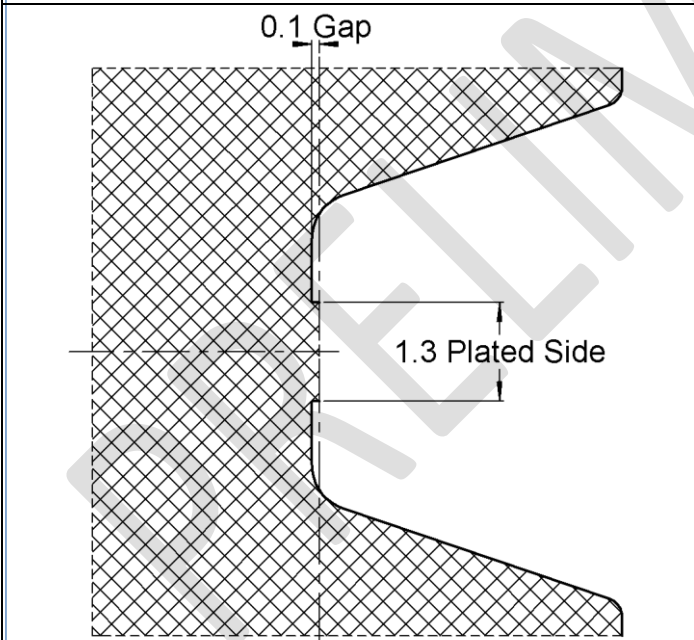
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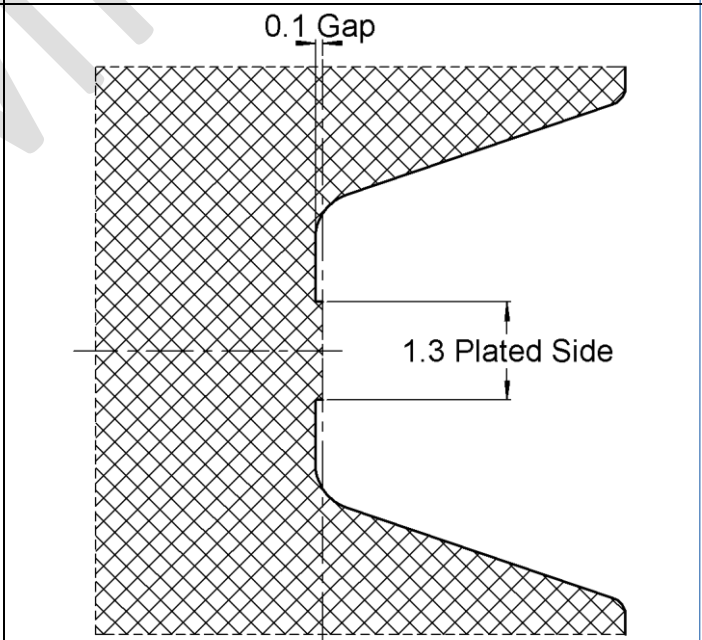
**Copper Layer 1**



**Copper Layer 2**



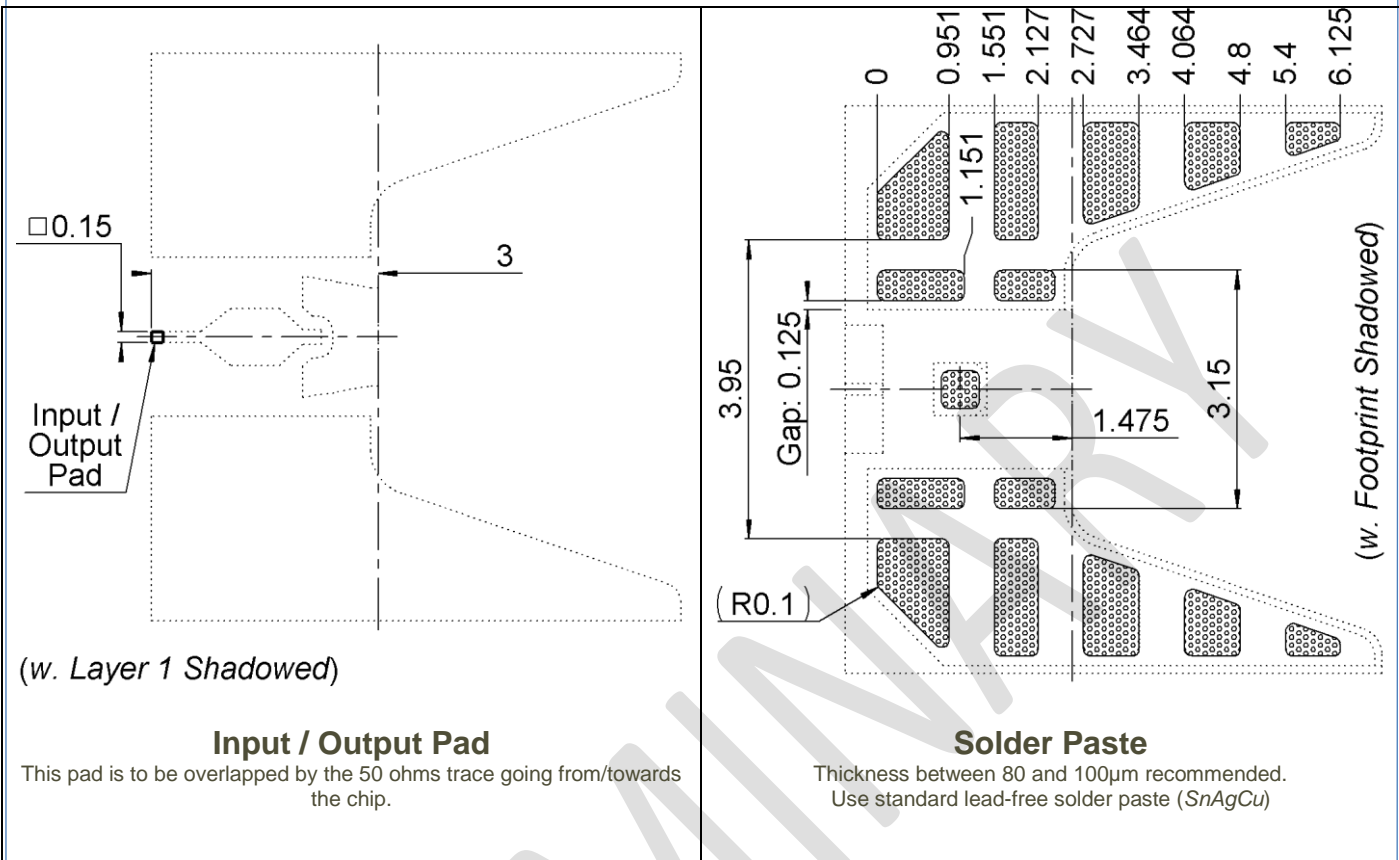
**Copper Layer 3**



**Copper Layer 4**

----- : The layer can expand beyond the footprint limit

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----- : The layer can expand beyond the footprint limit

See TDS for reflow instructions and temperature profile.  
 See attached DXF files (R12 version) for exact dimensions and vias position.

PRELIMINARY